# Low-Voltage 1.8/2.5/3.3V 16-Bit Transceiver

# With 3.6 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The 74VCX16245 is an advanced performance, non-inverting 16-bit transceiver. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems.

When operating at 2.5 V (or 1.8 V) the part is designed to tolerate voltages it may encounter on either inputs or outputs when interfacing to 3.3 V busses. It is guaranteed to be over–voltage tolerant to 3.6 V.

The VCX16245 is designed with byte control. It can be operated as two separate octals, or with the controls tied together, as a 16-bit wide function. The Transmit/Receive ( $T/\overline{R}n$ ) inputs determine the direction of data flow through the bi-directional transceiver. Transmit (active–HIGH) enables data from A ports to B ports; Receive (active–LOW) enables data from B to A ports. The Output Enable inputs ( $\overline{OEn}$ ), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

#### **Features**

- Designed for Low Voltage Operation: V<sub>CC</sub> = 1.65–3.6 V
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 2.5 ns max for 3.0 to 3.6 V

3.0 ns max for 2.3 to 2.7 V 6.0 ns max for 1.65 to 1.95 V

• Static Drive: ±24 mA Drive at 3.0 V

±18 mA Drive at 2.3 V ±6 mA Drive at 1.65 V

- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0 \text{ V}$
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V
- Pb-Free Package is Available\*



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TSSOP-48 DT SUFFIX CASE 1201

#### MARKING DIAGRAM

8



1

A = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
74VCX16245DT	TSSOP	39 / Rail
74VCX16245DTR	TSSOP	2500/Tape & Reel
74VCX16245DTRG	TSSOP (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

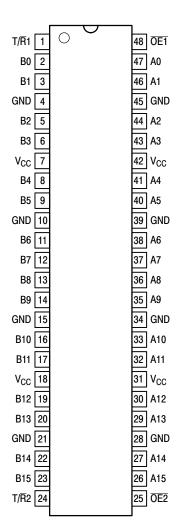


Figure 1. 48-Lead Pinout (Top View)

# A2-А3-A4 A5 A6 A7 · A8-Α9 A10 A11 · A12 A13 29 A14 27 A15-

T/R1

OE2 24 T/R2

48 OE1

25

A0 47

46 A1

44

43

41

40

38

37

36

35

33

32

30

26

Figure 3. IEC Logic Diagram

# **PIN NAMES**

Pins	Function
OEn	Output Enable Inputs
T/Rn	Transmit/Receive Inputs
A0-A15	Side A Inputs or 3–State Outputs
B0-B15	Side B Inputs or 3–State Outputs

T/R1 1 OET 48	T/R2 24 OE2 25
A0:7 B0:7	A8:15  One of Eight

Figure 2. Logic Diagram

2 B0

3 B1

5 B2

6 B3

9 B5

B4

В6

В7

13 B8

14 B9

16 B10

17 B11

19 B12

20 B13

22 B14 23 B15

8

11

12

1 ∇

2 ∇

3 ∇

4 ∇

EN1

EN2

EN3

EN4

Inp	uts	Outpute	Inp	outs	Outrote
OE1	T/R1	Outputs	OE2	T/R2	Outputs
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	Н	Bus A0:7 Data to Bus B0:7	L	Н	Bus A8:15 Data to Bus B8:15
Н	Х	High Z State on A0:7, B0:7	Н	Х	High Z State on A8:15, B8:15

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable

#### **ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +4.6		V
VI	DC Input Voltage	$-0.5 \le V_1 \le +4.6$		V
Vo	DC Output Voltage	$-0.5 \le V_O \le +4.6$	Output in 3–State	V
		$-0.5 \le V_{O} \le V_{CC} + 0.5$	Note 1.; Outputs Active	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	$V_{O} > V_{CC}$	mA
Io	DC Output Source/Sink Current	±50		mA
Icc	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

<sup>\*</sup> Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter		Min	Тур	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
VI	Input Voltage		-0.3		3.6	V
V <sub>O</sub>	Output Voltage	(Active State) (3-State)	0 0		V <sub>CC</sub> 3.6	V
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V				-24	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V				24	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.3V – 2.7V				-18	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.3V - 2.7V				18	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 1.65 – 1.95V				-6	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 1.65 – 1.95V				6	mA
T <sub>A</sub>	Operating Free-Air Temperature		-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to	2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V

<sup>1.</sup> I<sub>O</sub> absolute maximum rating must be observed.

#### DC ELECTRICAL CHARACTERISTICS

			T <sub>A</sub> = -40°0	C to +85°C	
Symbol	Characteristic	Condition	Min	Max	Unit
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	1.65V ≤ V <sub>CC</sub> < 2.3V	0.65 x V <sub>CC</sub>		V
		2.3V ≤ V <sub>CC</sub> ≤ 2.7V	1.6		
		2.7V < V <sub>CC</sub> ≤ 3.6V	2.0		
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	1.65V ≤ V <sub>CC</sub> < 2.3V		0.35 x V <sub>CC</sub>	V
		2.3V ≤ V <sub>CC</sub> ≤ 2.7V		0.7	
		2.7V < V <sub>CC</sub> ≤ 3.6V		0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	$1.65V \le V_{CC} \le 3.6V; I_{OH} = -100\mu A$	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 1.65V; I <sub>OH</sub> = -6mA	1.25		
		$V_{CC} = 2.3V; I_{OH} = -6mA$	2.0		
		V <sub>CC</sub> = 2.3V; I <sub>OH</sub> = -12mA	1.8		
		V <sub>CC</sub> = 2.3V; I <sub>OH</sub> = -18mA	1.7		
		$V_{CC} = 2.7V; I_{OH} = -12mA$	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		$V_{CC} = 3.0V; I_{OH} = -24mA$	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	$1.65V \le V_{CC} \le 3.6V; I_{OL} = 100\mu A$		0.2	V
		V <sub>CC</sub> = 1.65V; I <sub>OL</sub> = 6mA		0.3	
		$V_{CC} = 2.3V; I_{OL} = 12mA$		0.4	
		V <sub>CC</sub> = 2.3V; I <sub>OL</sub> = 18mA		0.6	
		$V_{CC} = 2.7V; I_{OL} = 12mA$		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 18mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	
lı	Input Leakage Current	$1.65V \le V_{CC} \le 3.6V; \ 0V \le V_{I} \le 3.6V$		±5.0	μΑ
l <sub>OZ</sub>	3-State Output Current	$1.65 \text{V} \leq \text{V}_{CC} \leq 3.6 \text{V}; \ 0 \text{V} \leq \text{V}_{O} \leq 3.6 \text{V}; \\ \text{V}_{I} = \text{V}_{IH} \text{ or } \text{V}_{IL}$		±10	μΑ
I <sub>OFF</sub>	Power-Off Leakage Current	$V_{CC} = 0V$ ; $V_I$ or $V_O = 3.6V$		10	μΑ
I <sub>CC</sub>	Quiescent Supply Current (Note 3.)	$1.65V \le V_{CC} \le 3.6V$ ; $V_I = GND \text{ or } V_{CC}$		20	μΑ
		$1.65V \le V_{CC} \le 3.6V; 3.6V \le V_{I}, V_{O} \le 3.6V$		±20	μΑ
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	$2.7V < V_{CC} \le 3.6V; V_{IH} = V_{CC} - 0.6V$		750	μΑ

- 2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.
- 3. Outputs disabled or 3-state only.

#### **AC CHARACTERISTICS** (Note 4.; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500\Omega$ )

					Lir	nits			
					T <sub>A</sub> = -40°	C to +85°C			
			V <sub>CC</sub> = 3.0	OV to 3.6V	V <sub>CC</sub> = 2.3	3V to 2.7V	V <sub>CC</sub> = 1.6	5 to1.95V	
Symbol	Parameter	Waveform	Min	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	1	0.8 0.8	2.5 2.5	1.0 1.0	3.0 3.0	1.5 1.5	6.0 6.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	2	0.8 0.8	3.8 3.8	1.0 1.0	4.9 4.9	1.5 1.5	9.3 9.3	ns
t <sub>PHZ</sub>	Output Disable Time From High and Low Level	2	0.8 0.8	3.7 3.7	1.0 1.0	4.2 4.2	1.5 1.5	7.6 7.6	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 5.)			0.5 0.5		0.5 0.5		0.75 0.75	ns

 <sup>4.</sup> For C<sub>L</sub> = 50pF, add approximately 300ps to the AC maximum specification.
 5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

#### **DYNAMIC SWITCHING CHARACTERISTICS**

			T <sub>A</sub> = +25°C	
Symbol	Characteristic	Condition	Тур	Unit
V <sub>OLP</sub>	Dynamic LOW Peak Voltage	$V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	0.25	V
	(Note 6.)	$V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	0.6	
		$V_{CC} = 3.3V$ , $C_L = 30pF$ , $V_{IH} = V_{CC}$ , $V_{IL} = 0V$	0.8	
$V_{OLV}$	Dynamic LOW Valley Voltage	$V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	-0.25	V
	(Note 6.)	$V_{CC} = 2.5V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	-0.6	
		$V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	-0.8	
V <sub>OHV</sub>	Dynamic HIGH Valley Voltage	$V_{CC} = 1.8V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	1.5	V
	(Note 7.)	$V_{CC} = 2.5V$ , $C_L = 30pF$ , $V_{IH} = V_{CC}$ , $V_{IL} = 0V$	1.9	
		$V_{CC} = 3.3V, C_L = 30pF, V_{IH} = V_{CC}, V_{IL} = 0V$	2.2	

<sup>6.</sup> Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

#### **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	Note 8.	6	pF
C <sub>OUT</sub>	Output Capacitance	Note 8.	7	pF
C <sub>PD</sub>	Power Dissipation Capacitance	Note 8., 10MHz	20	pF

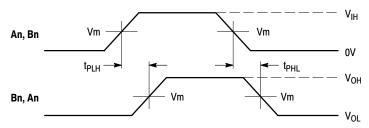
<sup>8.</sup>  $V_{CC}$  = 1.8, 2.5 or 3.3V;  $V_{I}$  = 0V or  $V_{CC}$ .

# AC CHARACTERISTICS ( $t_R = t_F = 2.0ns$ ; $C_L = 50pF$ ; $R_L = 500\Omega$ )

			Limits				
				T <sub>A</sub> = -40°C	C to +85°C		
			V <sub>CC</sub> = 3.0	0V to 3.6V	V <sub>CC</sub> :	= 2.7V	1
Symbol	Parameter	Waveform	Min	Max	Min	Max	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Input to Output	3	1.0 1.0	3.0 3.0		3.6 3.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time to High and Low Level	4	1.0 1.0	4.4 4.4		5.4 5.4	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time From High and Low Level	4	1.0 1.0	4.1 4.1		4.6 4.6	ns
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output-to-Output Skew (Note 9.)			0.5 0.5		0.5 0.5	ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

<sup>7.</sup> Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.



#### **WAVEFORM 1 - PROPAGATION DELAYS**

 $t_R$  =  $t_F$  = 2.0ns, 10% to 90%; f = 1MHz;  $t_W$  = 500ns

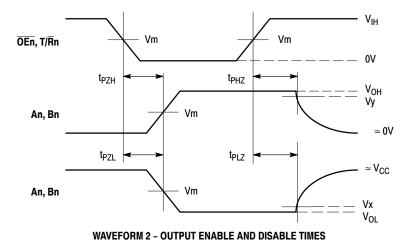
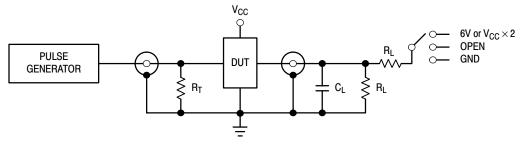


Figure 4. AC Waveforms

 $t_R = t_F = 2.0$ ns, 10% to 90%; f = 1MHz;  $t_W = 500$ ns

	V <sub>CC</sub>					
Symbol	3.3V ±0.3V	2.5V ±0.2V	1.8V ±0.15V			
V <sub>IH</sub>	2.7V	V <sub>CC</sub>	V <sub>CC</sub>			
V <sub>m</sub>	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2			
V <sub>x</sub>	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.15V	V <sub>OL</sub> + 0.15V			
V <sub>y</sub>	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.15V	V <sub>OH</sub> – 0.15V			

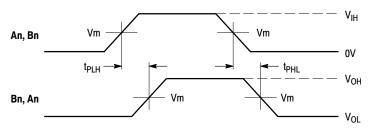


TEST	SWITCH	
t <sub>PLH</sub> , t <sub>PHL</sub>	Open	
t <sub>PZL</sub> , t <sub>PLZ</sub>	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$ ; 1.8V $\pm 0.15V$	
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND	

 $C_L = 30$ pF or equivalent (Includes jig and probe capacitance)

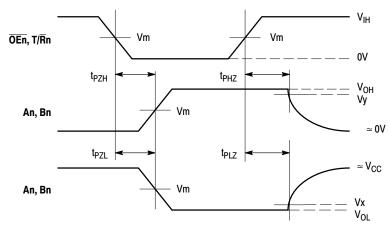
 $R_L = 500\Omega$  or equivalent  $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Figure 5. Test Circuit



#### **WAVEFORM 3 - PROPAGATION DELAYS**

 $t_R$  =  $t_F$  = 2.0ns, 10% to 90%; f = 1MHz;  $t_W$  = 500ns

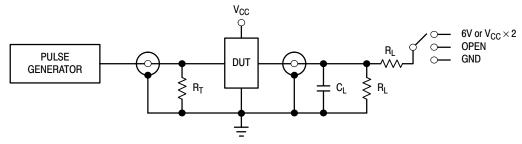


# WAVEFORM 4 - OUTPUT ENABLE AND DISABLE TIMES

 $t_R = t_F = 2.0$ ns, 10% to 90%; f = 1MHz;  $t_W = 500$ ns

Figure 6. AC Waveforms

	V <sub>CC</sub>		
Symbol	3.3V ±0.3V	2.7V	
V <sub>IH</sub>	2.7V	2.7V	
V <sub>m</sub>	1.5V	1.5V	
V <sub>x</sub>	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.3V	
V <sub>y</sub>	V <sub>OH</sub> – 0.3V	V <sub>OH</sub> – 0.3V	



TEST	SWITCH Open	
t <sub>PLH</sub> , t <sub>PHL</sub>		
t <sub>PZL</sub> , t <sub>PLZ</sub>	6V at $V_{CC}$ = 3.3 ±0.3V; $V_{CC} \times$ 2 at $V_{CC}$ = 2.5 ±0.2V; 1.8 ±0.15V	
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND	

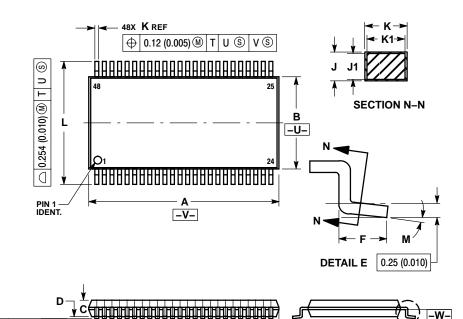
 $C_L = 50$ pF or equivalent (Includes jig and probe capacitance)

 $R_L = 500\Omega$  or equivalent  $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Figure 7. Test Circuit

#### PACKAGE DIMENSIONS

#### **TSSOP DT SUFFIX** CASE 1201-01 **ISSUE A**



- 1. DIMENSIONING AND TOLERANCING PER ANSI
- T 14.5WI, 1962.
  CONTROLLING DIMENSION: MILLIMETER.
  DIMENSIONS A AND B DO NOT INCLUDE
  MOLD FLASH, PROTRUSIONS OR GATE
  BURRS. MOLD FLASH OR GATE BURRS
- SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	12.40	12.60	0.488	0.496
В	6.00	6.20	0.236	0.244
С	-	1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
Н	0.37		0.015	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8°	0 °	8°

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